AMENDMENTS TO THE CLAIMS

1. (currently amended) A vertical multiple bit memory cell comprising:

a vertical metal oxide semiconductor field effect transistor (MOSFET) extending horizontally outward from a substrate, the MOSFET having a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain regions, and a gate separated from the channel region by a high dielectric constant gate insulator that can store a first charge in a first storage region and a second charge in a second storage region;

a negative bias connection coupled to the substrate that enhances hot electron injection;

a first transmission line coupled to the first source/drain region; and

a second transmission line coupled to the second source/drain region.

2. (canceled)

3. (Original) The cell of claim 1 wherein the MOSFET is operated with either the first source/drain region or the second source/drain region serving as the source region in response to a direction of operation of the MOSFET.

4. (Original) The cell of claim 1 wherein the MOSFET includes the first and second charges simultaneously programmed into both the first and second storage regions.

5. (Original) The cell of claim 1 wherein the first storage region is adjacent the first source/drain region, and wherein the second storage region is adjacent the second source/drain region.

6. (Original) The cell of claim 1 wherein the gate insulator includes a composite layer of oxide-nitride-aluminum oxide.

7. (Original) The cell of claim 1 wherein the gate insulator is comprised of two or more oxide materials selected from the group of silicon, titanium, tantalum, hafnium, and lanthanum.

8. (Original) A memory array, comprising:

a plurality of vertical multiple bit cells extending horizontally from a substrate and

separated by trenches, wherein each vertical multiple bit cell includes a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain regions, and a gate separated from the channel region by a gate insulator having a composite structure wherein the gate insulator has a first charge storage region and a second charge storage region, the substrate being coupled to a negative bias that enhances hot electron injection;

a number of first data lines coupled to the second source/drain region of each multiple bit cell along columns of the memory array;

a number of word lines coupled to the gate of each multiple bit cell along rows of the memory array; and

a number of second data lines coupled to the first source/drain region of each multiple bit cell along columns of the memory array.

9. (Original) The multiple bit cell of claim 8 wherein the first storage region is adjacent the first source/drain region, and the second storage region is adjacent the second source/drain region.

10. (Original) The multiple bit cell of claim 8 wherein the composite structure is comprised of oxide-nitride-aluminum oxide.

11. (Original) The multiple bit cell of claim 8 wherein the MOSFET includes a charge programmed in both the first storage region and the second storage region.

12. (Original) The multiple bit cell of claim 9 wherein the charges programmed in the first and second charge storage regions create a high voltage threshold when the MOSFET is operated with an adjacent first source/drain region or the second source/drain region serving as the source region.

13. (Original) An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes a memory array having a plurality of vertical memory cells, each vertical memory cell comprising:

a vertical metal oxide semiconductor field effect transistor (MOSFET) extending horizontally outward from a substrate, the MOSFET having a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain regions, and a

gate separated from the channel region by a high dielectric constant gate insulator that can store a first charge in a first storage region and a second charge in a second storage region, the substrate coupled to a negative bias to enhance hot electron injection;

a first transmission line coupled to the first source/drain region; and

a second transmission line coupled to the second source/drain region.

14. (Original) The system of claim 13 wherein the MOSFET includes both the first charge stored in the first storage region and the second charge stored in the second storage region.

15. (Original) The system of claim 13 wherein the gate insulator of each transistor includes a composite structure having a trapping layer selected from a group of oxides of hafnium and lanthanum.

16. (Original) A method for programming a vertical memory cell that extends horizontally outward from a substrate, the method comprising:

applying a first voltage to a first source/drain region of the vertical memory cell;

applying a second voltage to a second source/drain region of the vertical memory cell;

applying a gate voltage to a gate of the vertical memory cell; and

applying a negative voltage to the substrate of the vertical memory cell such that applying the first, second, gate, and negative substrate voltages to the vertical memory cell creates substrate enhanced hot electron injection into the gate insulator to program a charge into at least one of a first storage region and a second storage region in a gate insulator, the vertical memory cell operating with either the first source/drain region or the second source/drain region serving as the source region in response to the first and second voltages.

17. (Original) A method for erasing a vertical memory cell that extends horizontally outward from a substrate, the method comprising:

applying a positive voltage to at least one of a first source/drain region and a second source/drain region of the vertical memory cell;

applying a negative gate voltage to a gate of the vertical memory cell; and

applying a negative substrate voltage to the substrate of the vertical memory cell such that applying the positive, gate, and negative substrate voltages to the one or more vertical memory cells creates substrate enhanced hot hole injection into the gate insulator to erase a

charge from at least one of a first storage region and a second storage region in a gate insulator.

18. (Original) The method of claim 17 wherein the positive voltage is applied to both the first and the second source/drain regions.

19. (Original) The method of claim 17 wherein the negative gate voltage is larger than the negative substrate voltage.

20. (currently amended) A method for forming a vertical multiple bit memory cell, the method comprising:

forming a vertical metal oxide semiconductor field effect transistor (MOSFET) extending horizontally outward from a substrate, the MOSFET having a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain regions, and a gate separated from the channel region by a gate insulator, having a composite structure of two or more oxide materials selected from the group of silicon, titanium, tantalum, hafnium, or lanthanum, that is adapted to have a charge programmed in at least one of a first storage region and a second storage region in the gate insulator;

forming a first transmission line coupled to the first source/drain region; and

forming a second transmission line coupled to the second source/drain region.

21 - 23 (canceled)